Application Note 195
DSTINI1 (TINIm390) Verification Module Chipset Reference Design

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Much of the information contained in this application note is taken from the TINI Specification and Developer's Guide (www.maxim-ic.com/TINIguide).

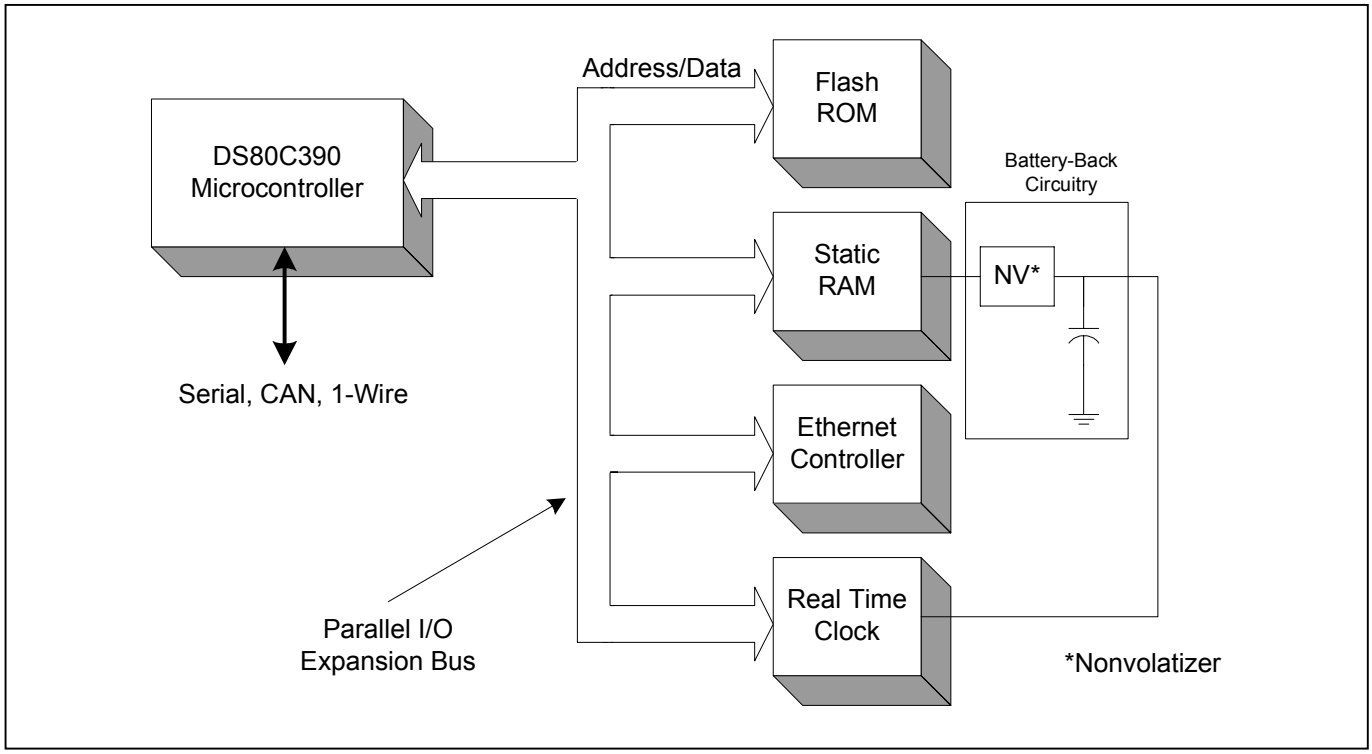
INTRODUCTION

The DSTINI®1 (TINIm390) Verification Module is an implementation of the TINI-390 Chipset Reference Design and can be used as a development tool for writing embedded web servers. It includes a 10Base-T Ethernet interface, 512kB of flash for critical system code, up to 1MB of static RAM, dual serial ports, a real-time clock (RTC), dual 1-Wire® ports, a CAN bus interface, and exposes the address and data bus of the DS80C390 microcontroller for simple system expansion. This application note provides a technical description of the TINIm390 Verification Module. The Verification Module schematic, bill of materials, and pinout are downloadable from our ftp site, ftp://ftp.dalsemi.com.

System Overview

A minimum TINI-390 chipset design must include the DS80C390 microcontroller, flash ROM, RAM, and a DS2502 IEEE MAC address chip. An expanded chipset design like the TINIm390 can include support for many more advanced features. Figure 1 shows a block diagram of the TINIm390 Verification Module.

Figure 1. TINIm390 Verification Module Block Diagram



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In addition to the functionality of a minimal chipset design, the TINIm390 also includes these important features:

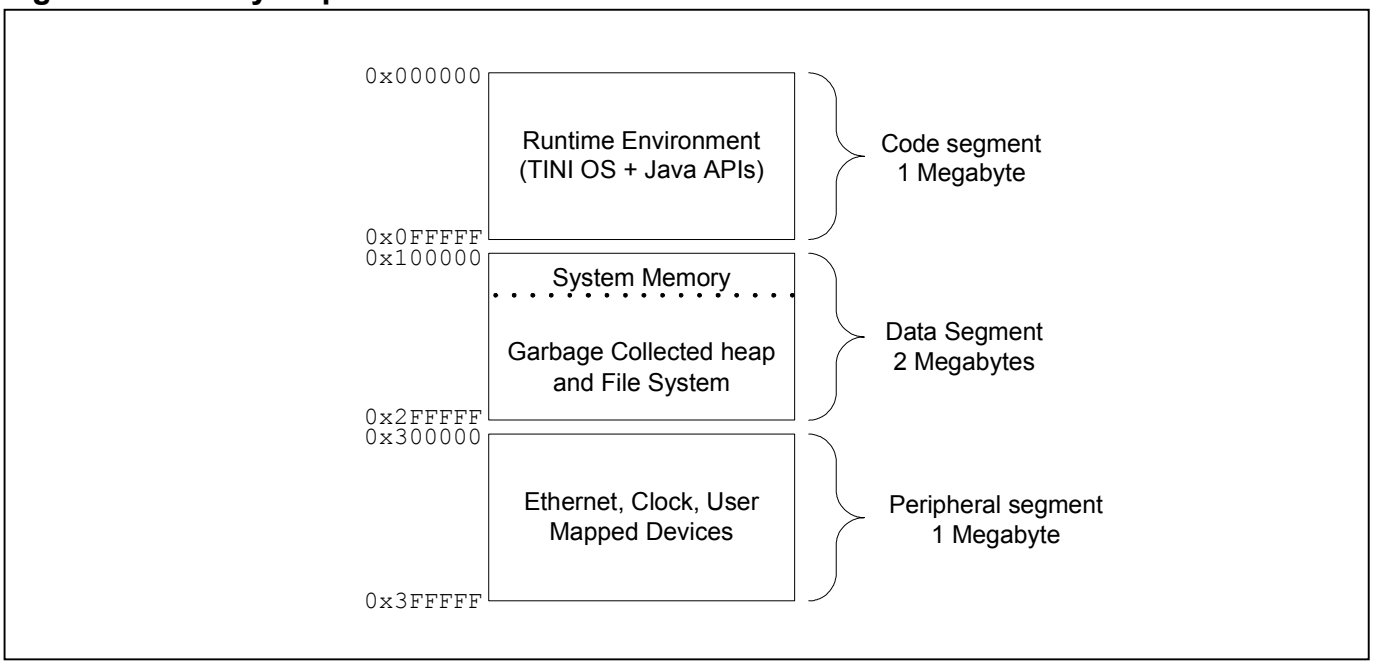
- 512kB of flash memory for critical system code
- 512kB/1MB of NV SRAM
- 10Base-T Ethernet Controller
- RTC
- Dual 1-Wire net interfaces
- Dual CAN controllers
- Dual serial ports (one RS-232 level and one +5V level)
- Exposes the microcontroller's address and data busses for parallel I/O expansion
- Requires only a single +5V power supply

Memory Description

The memory map specifies where memory and other peripheral devices are decoded in the microcontroller's address space. Figure 2 shows the TINIm390's memory map. It contains three distinct segments of code, data, and peripheral.

The maximum code segment is 1MB, the data segment maximum is 2MB, and the peripheral segment is up to 1MB. If only 512kB of flash ROM exists in the code segment, the starting address of the data segment remains 0x100000. In other words, the starting addresses of the segments always remain as shown in Figure 2.

Figure 2. Memory Map



Memory chips occupy the code and data segments, and other types of devices, including the Ethernet controller and the RTC, occupy the peripheral segment. Additional peripheral devices that support a parallel interface can be mapped in the peripheral space. However, adding hardware in this fashion also adds capacitive loading to either or both the data and address buses (depending on the device). The system designer must be aware of this loading to ensure reliable system operation. See Table 1 for temperature vs. load characteristics. When adding devices on the peripheral space, the address ranges of the Ethernet controller and the RTC must be avoided.

There is also a separate 4MB peripheral area, known as peripheral chip-enable (PCE) space, that can be used to interface large (up to four 1MB) external memory chips or other hardware devices directly to the microcontroller's address and data buses. However, most hardware is mapped in the peripheral segment because the controller can access it more efficiently. If no devices are mapped in the PCE space, the four PCE control pins can be used as general-purpose port pins.

Detailed memory timing diagrams can be found in the DS80C390 data sheet (www.maxim-ic.com/DS80C390). The TINI Runtime Environment uses two cycle $\overline{PCE0\text{-}3}$ data reads and writes.

Table 1. Typical Temperature vs. Load Characteristics

NUMBER OF LOADS*	MIN TEMPERATURE (ºC)	MAX TEMPERATURE (ºC)
0	-20	+70
1	-20	+70
2	-20	+70
3	-20	+60
4	-20	+55
5	-20	+50

**A load is characterized as 7pF applied to the address, control, and data lines of a TINIm390-512.*

TINIm390 Chipset Components

The TINI-390 chipset is composed of the Maxim/Dallas components on the TINIm390 Verification Module. These are standard components and can be purchased from Maxim direct. Data sheets for each of the components can be found on our website at www.maxim-ic.com. The components include the following:

- DS80C390 Microcontroller
- DS2502-E48 IEEE 1-Wire MAC Address
- DS2433 1-Wire Memory
- DS1315 Real-Time Clock
- DS1321 Nonvolatile RAM Controller

PIN DESCRIPTION

PIN	NAME	FUNCTION
1	IN3	TTL Input. Dual-purpose input pin that can be used as DCD for RTS/CTS flow control or as a general-purpose data input pin.
2	IN1	TTL Input. Dual-purpose input pin that can be used as CTS for RTS/CTS flow control or as a general-purpose data input pin.
3–7	GND	Digital Circuit Ground
8	OWIO	1-Wire Input/Output Pin. 1-Wire bus with slew-rate-controlled pulldown, active pullup, ability to switch in V_{PP} to program EPROM, and ability to switch in V_{DD} through a low-impedance path to program EEPROM or to perform a temperature conversion.
9	V_{PP}	+12V Supply Input for EPROM Programming (Note 1)
10	CTX	CAN Bus Tx Line or Bidirectional Port Pin
11	CRX	CAN Bus Rx Line or Bidirectional Port Pin
12	$\overline{CE0}$	CPU Chip Enable 0 (Note 2)
13	A19	Address Lines (Note 3)
33–36	A7–A4	
37–44	A8–A15	
54–57	A0–A3	
60–62	A16–A18	
14	TX1	Serial Port 1 Output TTL
15	XRX1	Serial Port 1 Input TTL
16	$\overline{RD}$	CPU Read Strobe (Note 3)
17	INTOW	Internal 1-Wire Bus (Note 4)
18	SMCRST	Peripheral Reset from CPU
19	TX232	Serial Port 0 Output
20	RX232	Serial Port 0 Input
21	TX	Serial Port 0 Output TTL
22	XRX0	Serial Port 0 Input TTL
23	$\overline{EXTINT}$	CPU Interrupt Input
24	CPURST	CPU Reset Input (Note 5)
25	DTR232	RS232 CPU Reset Input (Note 6)
26	EN2480	On-Board DS2480 Enable
27	$\overline{PCE3}$	Peripheral Chip Enables from CPU (Note 3)
28	$\overline{PCE2}$	
29	$\overline{PCE1}$	
30	$\overline{PEC0}$	
31	$\overline{CE3}$	Chip Enable 3 from CPU (Note 3)
32	$\overline{PSEN}$	Program Store Enable from CPU (Note 3)
45	$\overline{RCE0}$	CE0 Return to On-Board Flash ROM (Note 2)
46–53	D7–D0	Data Lines (Note 3)
58	$\overline{WR}$	CPU Write Strobe (Note 3)
59	IN2	TTL Input. This pin can be used as general-purpose input port pin.
63	ETH3	10Base-T Differential Inputs
64	ETH6	
65	ETH2	10Base-T Differential Outputs
66	ETH1	
67–70	V_{CC}	±5% at 250mA (max), +5V DC (Note 7)
71	OUT1	TTL Output. Dual-purpose output pin that can be used as RTS for RTS/CTS flow control or as a general-purpose data output pin.
72	OUT2	TTL Output. Dual-purpose output pin that can be used as DTR for RTS/CTS flow control or as a general-purpose data output pin.

Note 1: Pin 9 (V_{PP}) may be connected to +12V DC to allow EPROM programming with the on-board DS2480. If pin 9 (V_{PP}) is not used in this manner, it must be connected to V_{CC}.

Note 2: To execute from the on-board flash ROM, connect $\overline{CE0}$ (Pin 12) to $\overline{RCE0}$ (Pin 45). If an external boot-up memory is provided, $\overline{RCE0}$ must be pulled high (V_{CC}) to disable the on-board flash ROM or data bus interference could occur. Logic in the $\overline{CE0}$ to $\overline{REC0}$ path must take care to present minimal delay (<6ns) to the $\overline{CE0}$ signal.

Note 3: Address bus, data bus, and strobe lines are subject to strict loading limitations. Exceeding these limits can cause erratic system operation with on-board as well as off-board resources. Be sure to buffer any signals that will be heavily loaded off-board. Always adhere to the design specifications to assure reliable system operation.

Note 4: The internal 1-Wire bus (INTOW) is a microcontroller port pin that drives the CPU status LED and links to the board's 1-Wire EPROM memory chip that contains the TINIm390's Ethernet MAC address. Other 1-Wire devices may be connected to this bus in the future to convey configuration data to the TINIm390. If this bus is shorted to ground (low) during system boot-up, a Master Clear is invoked. This forces the contents of the SRAM to be reinitialized.

Note 5: CPURST must be taken high (V_{CC}) and then released to cause a reset of the TINIm390. An active state on the DTR232 (pin 25) also takes this line high. This line is pulled down through a 22kΩ pulldown on-board.

Note 6: The RS232-level DTR control line is used to invoke a TINIm390 reset when asserted. This is to facilitate loaders and diagnostic equipment that must invoke a reset of the board to gain control of the system. This line is pulled to -8V through 22kΩ and has a 0.01μF capacitor filter to prevent cross talk on an open DTR conductor from causing spurious resets of the TINIm390 if this function is not used.

Note 7: TINI board power consumption is rated at no more than 250mA.

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin Relative to Ground Except for the Following Pins:	-0.3V to V_{CC} + 0.3V
V_{PP}	+14V
INTOW	+14V
RX232	±30V
ETH3, ETH6	+125V
ETH2, ETH1	+125V
Operating Temperature	-40°C to +85°C
Storage Temperature	-55°C to +85°C
Soldering Temperature	See IPC/JEDEC J-STD-020A

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = -20°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Voltage	V_{CC}		4.75	5.00	5.25	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75 to 5.25V, T_A = -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{CC}		4.75		5.25	V
Output Low Voltage	V_{OL}	I_{OL} = 1.7mA			0.40	V
Output High Voltage	V_{OH}	-680μA	2.4			V
Input Low Voltage	V_{IL}		0		0.80	V
Input High Voltage	V_{IH}		2.2		V_{CC}	V
Input Leakage Current	I_{IL}	0.45 < V_{IN} < V_{CC}			320	μA
Reset Trip Point	V_{RST}		4.50		<4.75	V
Supply Current Active Mode	I_{CC}			250		mA
Output Low Voltage for Port 3, 5	V_{OL1}	I_{OL} = 1.6mA			0.45	V
Output Low Voltage for Port 3, 5	V_{OL2}	I_{OL} = 3.2mA			0.45	V
Output High Voltage for Port 3, 5	V_{OH1}	I_{OH} = -50μA	2.4			V

DC ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = 4.75 to 5.25V, T_A = -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage for Port 3, 5	V_{OH2}	I_{OH} = -1.5mA	2.4			V
Logic 1-to-0 Transition Current for Port 3, 5	I_L		-300		+300	µA
Input Current for IN1, IN2, IN3	I_{IH}			+75	+150	µA
Output Low Voltage for OUT1, OUT2	V_{OL3}	I_{OL} = 4mA			0.4	V
Output High Voltage for OUT1, OUT2	V_{OH3}	I_{OH} = -2mA	2.4			V
Output Leakage Current for OUT1, OUT2	I_{OL3}	0 < V_{IN} < V_{CC}	-10		+10	µA

AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 4.75 to 5.25V, T_A = -20°C to +70°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
External Oscillator Frequency	$1/t_{CLCL}$			18.432		MHz
$\overline{PSEN}$ Pulse Width	t_{PLPH}		0.5 t_{MCS} - 5			ns
$\overline{PSEN}$ Low to Valid Instruction In	t_{PLIV}				0.5 t_{MCS} - 20	ns
Input Instruction Hold after $\overline{PSEN}$	t_{PXIX}		0			ns
Input Instruction Float after $\overline{PSEN}$	t_{PXIZ}				See MOVX Characteristics	ns
Capacitive Load Presented to External Devices	C_L				90	pF
Expected Data Retention Time	t_{DR}	(Note 1)	10			Years

Note 1: The minimum expected data retention time in the absence of V_{CC} is 10 years at +25°C.
Note 2: All signals characterized with load capacitance of 80pF except $\overline{PSEN}$, $\overline{RD}$, and $\overline{WR}$ with 100pF.
Note 3: Specifications assume a 50% duty cycle for the oscillator.
Note 4: t_{MCS} is defined as 2 x t_{CLCL}.
Note 5: The value t_{MCS} is a function of the machine cycle clock in terms of the processor's input clock frequency. These relationships are described in the *Stretch Value Timing* table in the DS80C390 data sheet.

HANDLING INSTRUCTIONS

Handle the TINIm390 as if it were a PC-style memory module. The TINIm390 is designed to be robust, however electrostatic discharge (ESD) precautions should be observed when handling this module. As with any other electronic device with exposed circuitry, the TINIm390 should be stored in an anti-static box. When inserting the TINIm390 into a socket, verify that power is not present. V_{CC} and GND connections should be checked before applying power. Also, verify that the input power is between 4.75V and 5.25V.

MORE INFORMATION

Refer to the DS80C390 data sheet (www.maxim-ic.com/DS80C390) for detailed timing information on the microcontroller. Download the TINIm390_Tech.zip at ftp://ftp.dalsemi.com/pub/tini/appnotes/AN195.